DOCUMENT-IDENTIFIER: US 20050003599 A1

TITLE: Mosfet device with a strained channel

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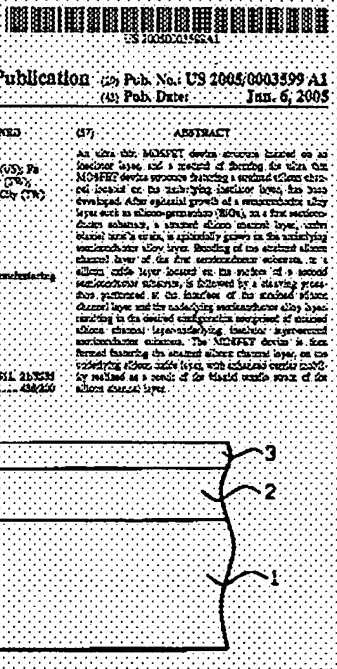
Abstract Paragraph - ABTX (1):
An ultra thin MOSFET device structure located on an insulator layer, and a method of forming the ultra thin MOSFET device structure featuring a strained silicon channel located on the underlying insulator layer, has been developed. After epitaxial growth of a semiconductor alloy layer such as silicon-germanium (SiGe), on a first semiconductor substrate, a strained silicon channel layer, under biaxial tensile strain, is epitaxially grown on the underlying semiconductor alloy layer. Bonding of the strained silicon channel layer of the first semiconductor substrate, to a silicon oxide layer located on the surface of a second semiconductor substrate, is followed by a cleaving procedure performed at the interface of the strained silicon channel layer and the underlying semiconductor alloy layer, resulting in the desired configuration comprised of strained silicon channel layer-underlying insulator layer-second semiconductor substrate. The MOSFET device is then formed featuring the strained silicon channel layer, on the underlying silicon oxide layer, with enhanced carrier mobility realized as a result of the biaxial tensile strain of the silicon channel layer.

Summary of Invention Paragraph - BSTX (7):
[0006] Performance optimization of an ultra thin body MOSFET device is possible through the use of a strained channel region, where the strain modifies the band structure of the channel region resulting in enhanced carrier transport properties. However the implementation of a MOSFET device on an insulator structure, featuring a strained channel region is difficult to achieve via conventional processes, and therefore not previously addressed. The present invention will however describe a novel fabrication process sequence is which a silicon channel region, under biaxial tensile strain, is successfully employed as a component for a MOSFET device, where the silicon channel region is located in a thin silicon layer which in turn is located on an insulator structure. Prior art such as: Kibbel et al, in U.S. Pat. No. 6,313,016; Liaw et al, in U.S. Pat. No. 5,891,769; Chu et al, in U.S. Pat. No. 5,906,951; Fitzgerald et al, in U.S. Pat. No. 6,291,321; and Leoues et al, in U.S. Pat. No. 5,659,187; have described methods of forming strained semiconductor and semiconductor alloys, on insulator structures. These prior arts however do not describe the novel process sequence used in this present invention, in which a thin, strained silicon layer is obtained on an underlying insulator structure.

Summary of Invention Paragraph - BSTX (10):
[0008] It is another object of this invention to form a strained channel in a silicon layer under biaxial tensile strain, obtained via growth of the silicon layer on an underlying relaxed layer or substrate with a natural lattice constant larger than that of silicon.



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Yeo et al. (43) Pub. Date: Jan. 6, 2005

(54) MOSFET DEVICE WITH A STRAINED CHANNEL

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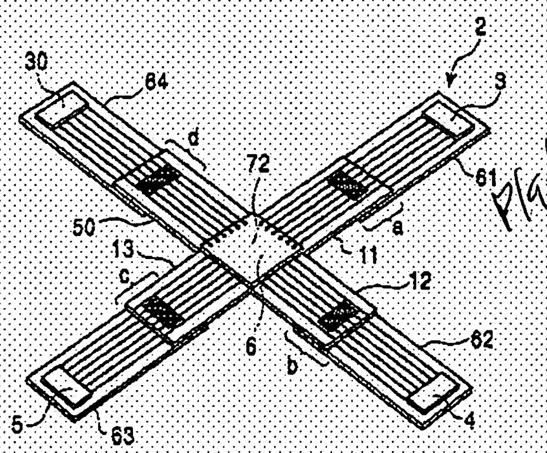
(57) ABSTRACT

An ultra thin MOSFET device structure located on an insulator layer, and a method of forming the ultra thin MOSFET device structure featuring a strained silicon channel located on the underlying insulator layer, has been developed. After epitaxial growth of a semiconductor alloy layer such as silicon-germanium (SiGe), on a first semiconductor substrate, a strained silicon channel layer, under biaxial tensile strain, is epitaxially grown on the underlying semiconductor alloy layer. Bonding of the strained silicon channel layer of the first semiconductor substrate, to a silicon oxide layer located on the surface of a second semiconductor substrate, is followed by a cleaving procedure performed at the interface of the strained silicon channel layer and the underlying semiconductor alloy layer, resulting in the desired configuration comprised of strained silicon channel layer-underlying insulator layer-second semiconductor substrate. The MOSFET device is then formed featuring the strained silicon channel layer, on the underlying silicon oxide layer, with enhanced carrier mobility realized as a result of the biaxial tensile strain of the silicon channel layer.

FIG. 2



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(54) LAMINATE TYPE SEMICONDUCTOR APPARATUS

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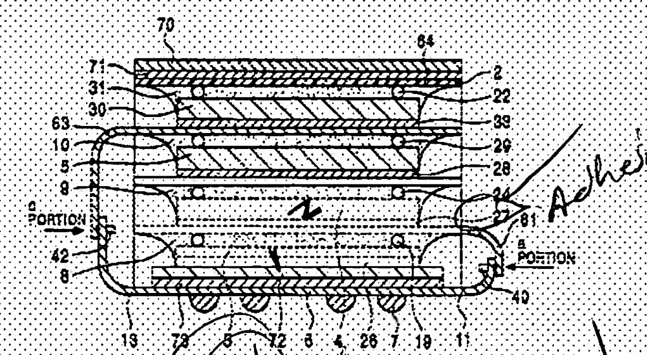
(57) ABSTRACT

A laminate-type semiconductor apparatus utilizing a flexible substrate being mounted with a plurality of semiconductor devices, in which the laminate-type semiconductor apparatus is free from incurring heat-radiation problem and has a fully leveled connection parts with sufficiently durable strength whereby distinctively compatible with high-density mounting thereof. More particularly, the present invention provides a laminate-type semiconductor apparatus which comprises a foldable flexible substrate mounted with a plurality of laminated semiconductor devices thereon, in which the foldable flexible substrate is folded so that plurality of semiconductor-device mounting areas of the substrate are mutually superposed whereby forming a laminate structure of semiconductor-device mounting areas thereon. An externally connected terminal disposing area disposed with a plurality of externally connected terminals is formed on one surface thereof. In addition, a reinforcing plate is secured to the side of the externally connected terminal disposing area via a material portion (adhesive agent) having stress relaxing function. Further, a heat-radiating plate is secured onto a surface on the opposite side from the externally connected terminal disposing area.



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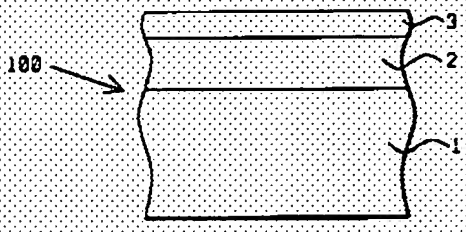
(57) ABSTRACT

An ultra thin MOSFET device structure located on an insulator layer, and a method of forming the ultra thin MOSFET device structure featuring a strained silicon channel located on the underlying insulator layer, has been developed. After epitaxial growth of a semiconductor alloy layer such as silicon-germanium (SiGe), on a first semiconductor substrate, a strained silicon channel layer, comprised with a thin, is epitaxially grown on the underlying semiconductor alloy layer. Bonding of the strained silicon channel layer of the first semiconductor substrate to a silicon oxide layer located on the surface of a second semiconductor substrate, is followed by a stacking process performed to the interface of the strained silicon channel layer and the underlying semiconductor alloy layer, resulting in the desired configuration comprised of strained silicon channel layer-underlying insulator layer-second semiconductor substrate. The MOSFET device is then formed featuring the strained silicon channel layer, on the underlying silicon oxide layer, with enhanced carrier mobility realized as a result of the tensile strained silicon channel layer.



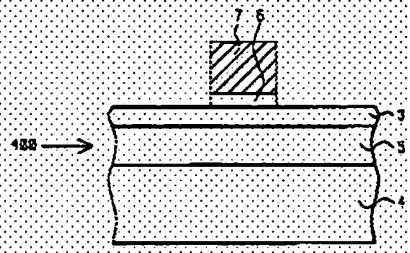


FIG. 5

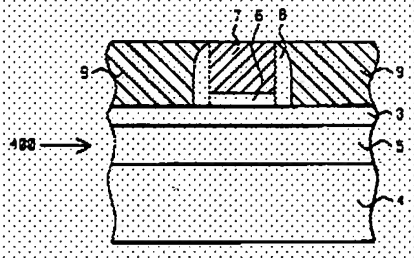


FIG. 6

complete the fabrication of a ultra thin MOSFET device, featuring a silicon channel region under biaxial tensile strain, on an underlying insulator structure.

Brief Description of Drawings Paragraph - DRTX (3):

[0012] FIGS. 1-6, which schematically, in cross-sectional style, describe key stages used to fabricate an ultra thin MOSFET device, featuring a silicon channel region under biaxial tensile strain, located directly on an underlying insulator structure.

Detail Description Paragraph - DETX (2):

[0013] The method of fabricating a MOSFET device, featuring a thin silicon channel under biaxial strain, located on an underlying insulator structure, will now be described in detail. A first semiconductor substrate 1, comprised of single crystalline silicon, with a <100> crystallographic orientation, is provided and shown schematically in FIG. 1. A material comprised with a natural lattice constant greater than that of silicon is next formed on first semiconductor substrate 1. The natural lattice constant of a material is its lattice constant in the relaxed state. Layer 2, a material with a natural larger lattice constant than that of silicon, can be a silicon-germanium (SiGe), layer, or a silicon-germanium-carbon (SiGeC) layer. The SiGe option is accomplished via epitaxial growth at a temperature between about 400 to 800.degree. C., using silane, or disilane as a source for silicon, while using germane as a source for germanium. The thickness of SiGe layer 2, is between about 0.1 to 10 microns, with a fraction of germanium between about 0.05 to 0.8. The growth conditions used for layer 2, result in a relaxed SiGe layer on silicon semiconductor substrate 1. If desired layer 2, can be comprised of SiGeC, again obtained via epitaxial growth conditions at a temperature between about 400 to 800.degree. C. Again silane, or disilane, and germane are used as reactants, with the addition of a hydrocarbon as a source for carbon. Layer 2, comprised of SiGeC, at a thickness between about 0.1 to 10 microns, is comprised with a germanium content between about 5 to 80%, and with a carbon content between about 0 to 4%, with the SiGeC layer again being in a relaxed condition. Therefore first wafer 100, shown schematically in FIG. 1, is now comprised of a relaxed layer 2, on semiconductor substrate 1.

Detail Description Paragraph - DETX (5):

[0016] Referring to third wafer 300, a large strain gradient exists at the interface between strained silicon layer 3, and relaxed semiconductor alloy, or SiGe layer 2. The large strain gradient allows a cut or a cleave to be accomplished at this interface resulting in the desired SOI configuration presented by fourth wafer 400, comprised of strained silicon layer 3, on insulator layer 5, with the SOI region residing on semiconductor substrate 4. The combination of a thin silicon layer, under biaxial tensile strain, on an insulator layer, provides the configuration needed to fabricate the ultra thin MOSFET device featuring enhanced carrier mobility in the stained channel region, with a reduced risk of short channel effects a result of the thin silicon layer overlying an insulator layer. This is

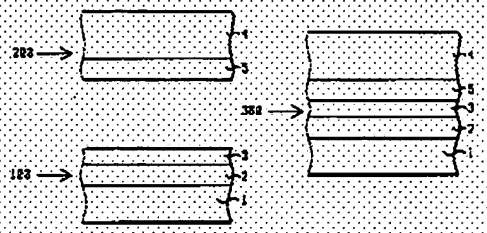


FIG. 3

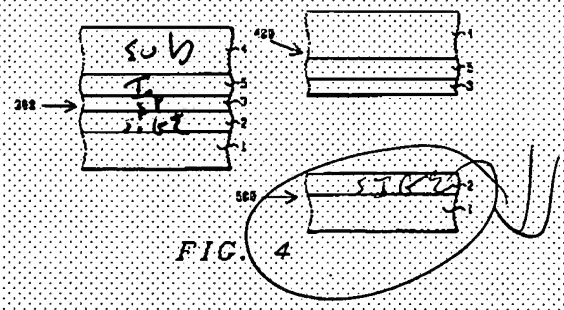


FIG. 4

the curly brackets 410. In the SiGe layer the amorphous region goes from the interface with the Si layer, a first interface, up to a second interface which is between the amorphous and crystalline portions of the SiGe layer. The top portion of the SiGe layer is not amorphized and remains monocrystalline.

[0030] FIG. 5 shows a schematic cross sectional view of the initial stage of re-crystallization by solid phase epitaxy. As the structure is being annealed the amorphized portion of the layered structure 410 is shrinking. The re-crystallization growth, indicated by arrows 510, propagates downwards from its original seeding place on the second interface, where the SiGe crystalline layer had a second lattice constant which was larger than the first lattice constant of the Si layer. As shown in FIG. 5, part of the SiGe layer 110' and Si layer 100' are still amorphous. The crystalline top portion of the SiGe layer is now extending downwards. In the case of a graded SiGe film the crystalline SiGe layer is no longer relaxed, having taken on the lattice constant of the second interface. Hence the strained crystalline SiGe layer is annotated as layer 520.

[0031] FIG. 6 shows a schematic cross sectional view of the layered structure after re-crystallization, wherein the Si layer has acquired a tensile strain. The part of the SiGe layer which was amorphized is now strained, which is indicated with the new annotation 520 referring to the whole layer. In this figure the Si layer is being forced to comply with the second lattice constant, and is acquiring a tensile strain. It has become the tensilely strained silicon-on-insulator 600. With this, the method for introducing the tensile strain in the silicon-on-insulator layer is complete. To fabricate a silicon-on-insulator layer that can be used to house devices and circuits, one has to remove the SiGe layer from the top of the strained Si layer. Methods for such removal are known in the art, and are typically done by selective etching, such as with 1HF: 2H.sub.2O.sub.2: 3CH.sub.3COOH. The use of a selective SiGe etchant is especially useful with a relaxed SiGe film having a uniform Ge concentration that extends down to the SiGe/Si interface (which is typically the case when the relaxed SiGe layer is made by the implantation and anneal method). With graded SiGe buffer layers it is some time preferable to incorporate a stop-etch layer or marker at the SiGe/Si interface. For example a boron delta-doping is sometime used as a stop-etch layer for both wet and dry etching.

[0032] FIG. 7 shows a schematic cross sectional view of the silicon-on-insulator wafer with the strained Si layer. The strained SiGe layer 520 has been removed, leaving the strained Si layer 600 exposed on the surface.

Cohen et al.

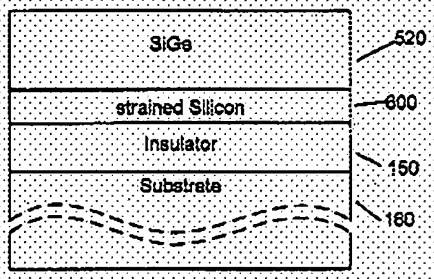


Fig. 6

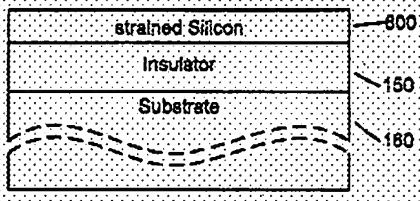


Fig. 7

illustrates a step in
which a photoresist layer 34 is deposited and a
lithographic process is
performed to open a window 36 in the area where gate
structure 14 will later be
formed. In an exemplary embodiment, germanium,
silicon, xenon, or any
amorphosizing species are implanted through window 36
and into substrate 12.
This amorphization implant amorphizes back gate region
38. Preferably,
germanium ions are provided at a very heavy dose (e.g.,
5.times.10.sup.14
-5.times.10.sup.15 cm.sup.-2). After the amorphization
implant, arsenic,
phosphorous, or any such species of N-type dopant is
implanted through the
window 36 and into substrate 12. Alternatively, P-type
dopant implants may be
used. The dopant implant provides a doping of back
gate region 38 in substrate
12. Region 38 can be a heavily doped P or N region (N+
or P+). Region 38 is
50-200 nm deep and 100-500 nm wide and designated by a
dashed area in FIGS.
6-8.

(11) IN FIG 7, a cross-sectional view of portion 10
illustrates a step in
which photoresist layer 34 is removed and an amorphous
silicon layer 40 is
deposited over oxide layer 22 and substrate 12. In one
embodiment, the
amorphous silicon layer 40 has a thickness of 100-300
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at a temperature of 450-500C. The opening in oxide
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which portion 10 is exposed to laser energy, such as an
excimer laser beam
having a 308 nm wavelength. The laser energy melts
amorphous silicon layer 40
and amorphous silicon region 38 due to the low melting
point of amorphous
silicon as compared with adjacent crystalline silicon
substrate 12.
Alternatively, other annealing and rapid thermal
annealing (RTA) processes can
be utilized.

(13) In FIG. 9, a cross-sectional view of portion 10
illustrates a step in
which, after the laser energy is removed, amorphous
silicon layer 40 and
amorphous back gate region 38 become recrystallized.
Recrystallization occurs
when amorphous regions 38 and 40 are transformed into
regions with a crystal
structure matching that of adjacent crystalline
substrate 12. The driving
force for this recrystallization is the difference in
internal energy between
the melted amorphous regions 38 and 40 and adjacent
crystalline substrate.
Amorphous silicon layer 40 is separated from substrate
12 by oxide layer 22.
The opening in oxide layer 22 operates as a seeding
window which allows the
amorphous silicon layer 40 to contact substrate 12,
thereby providing the
driving force in the form of differential internal
energy for recrystallization
of silicon layer 40.

(14) The N+ dopant present in amorphous silicon
region 38 becomes well
activated due to the melting and recrystallization
process. Subsequent to
recrystallization, region 38 becomes back gate region

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Generally, the gate conductor can be a metal, a polysilicon, or a polysilicon/germanium (SiXGe(1-x)) material that controls charge carriers in a channel region between the drain and the source to turn the transistor on and off. The transistors can be N-channel MOSFETs or P-channel MOSFETs.

Generally, it is desirable to manufacture smaller transistors to increase the component density on an integrated circuit. It is also desirable to reduce the size of integrated circuit structures, such as vias, conductive lines, capacitors, resistors, isolation structures, contacts, interconnects, etc. For example, manufacturing a transistor having a reduced gate length (a reduced width of the gate conductor) can have significant benefits. Gate conductors with reduced widths can be formed more closely together, thereby increasing the transistor density on the IC. Further, gate conductors with reduced widths allow smaller transistors to be designed, thereby increasing speed and reducing power requirements for the transistors.

Heretofore, lithographic tools have been utilized to form transistors and other structures on the integrated circuit. For example, lithographic tools can be utilized to define gate conductors, active lines, conductive lines, vias, doped regions, and other structures associated with an integrated circuit. Most conventional lithographic fabrication processes have only been able to define structures or regions having a dimension of 100 nm or greater.

In one type of conventional lithographic fabrication process, a photoresist mask is coated over a substrate or a layer above the substrate. The photoresist mask is lithographically patterned by providing electromagnetic radiation, such as, ultraviolet light, through an overlay mask. The portions of the photoresist mask exposed to the electromagnetic radiation react (e.g. are cured). The uncured portions of the photoresist mask are removed, thereby creating a photoresist mask having a pattern transposed from the pattern associated with the overlay. The patterned photoresist mask is utilized to etch other mask layers or structures. The etched mask layer and structures, in turn, can be used to define doping regions, vias, lines, etc.

As the dimensions of structures or features on the integrated circuit reach levels below 100 nm or even 50 nm, lithographic techniques are unable to precisely and accurately define the feature. For example, as described above, reduction of the width of the gate conductor (the gate length) associated with a transistor or the active line associated with an SOI transistor has significant beneficial effects. Future designs of transistors may require that the active line have a width of less than 50 nanometers.

Double-gate SOI MOSFET technology has received significant attention because of its advantages related to high drive current and high immunity to short channel effects. A double-gate MOSFET structure (FinFet) is discussed in "Sub 50-nm FinFet: PMOS," by Huang et al., International Electron Devices Meeting 1999. In addition, U.S. Pat. No. 5,889,302, issued to the assignee of the present application on Mar. 30, 1999, discusses a quadruple-gate field effect transistor on an SOI substrate. The double-gate MOSFET and quadruple-gate MOSFET are able to increase the drive current because the gate surrounds the active region by more than one layer (e.g., the effective gate total width is increased due to the double or quadruple gate structure). However, patterning narrow, dense active regions is challenging. As discussed above with respect to gate conductors, conventional lithographic tools are unable to accurately and precisely define active regions as structures or features with dimensions below 100 nm or 50 nm.